SPECIFICATION

Please replace paragraph [0018] with the following wherein strikethroughs denote deletions and underlines denote insertions:

[0018] Figure 1 shows a sense amplifier ("SA") in accordance with an exemplary embodiment of the invention. As shown, the SA 10 comprises a regenerative latch 11 coupled to an input differential transistor pair. The regenerative latch comprises N-channel field effect transistors ("nFETs") or NMOS transistors 36,38 and P-channel field effect transistors ("pFETs") or PMOS transistors 20-34. The input differential transistor pair comprises nFET transistors 12 and 14 and receives differential input signals INP and INN. The nFET transistor 16 comprises a clocked current source that alternatively enables and disables the differential transistor pair 12, 14. The R and S signals represent differential output signals from the SA and are generated by the regenerative latch 11 and latched by SR latch 40. As shown, the regenerative latch 11 generally comprises a pair of cross-coupled PMOS transistors 22 and 28, a pair of cross-coupled NMOS transistors 38 and 38, and a clocking circuit (which generally comprises PMOS transistors 24, 26, 32 and 34). PMOS transistors 20 and 30 also generally form a precharge circuit.